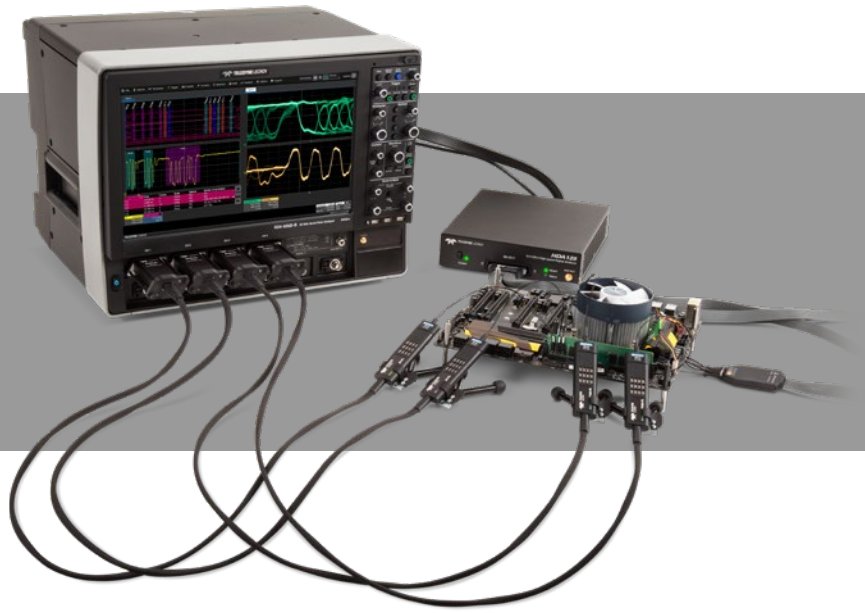
TELEDYNE LECROY
Everywhereyoulook™

DDR Debug Toolkit



Key Features

Read/Write burst separation with a push of a button

Simultaneous analysis of four different measurement views

View up to 10 eye diagrams with mask testing and eye measurements

Searchable Bus State views with intuitive color-coded overlays

Command bus based triggering

Perform jitter analysis for root cause analysis

Quickly configure measurements specific to DDR

Analyze specific regions of bursts with configurable qualifiers

Support for DDR2/3/4/5 and LPDDR2/3/4/4X

Select standard and custom speed grades

Most oscilloscope-based DDR physical layer test tools are targeted exclusively at JEDEC compliance testing, whereas the DDR Debug Toolkit provides test, debug, and analysis tools for the entire DDR design cycle. The unique DDR analysis capabilities provide automatic Read and Write burst separation, bursted data jitter analysis, and DDR-specific measurement parameters. All this DDR analysis can be performed simultaneously over four different measurement views.

Effortless Burst Separation

Easily separate Read and Write bursts with a push of a button for quick analysis and system validation. The multi-measurement view architecture provides flexibility when configuring measurements and allows for eye, jitter, and DDR measurements to be calculated on Read and Write bursts simultaneously.

Display Up to 10 Eye Diagrams

Gain a quick understanding of system performance by viewing up to 10 eye diagrams simultaneously. Overlay eye diagrams to visually inspect for skew, timing and jitter issues.

DDR-Specific Jitter Analysis

Effortlessly identify sources of jitter on bursted DDR signals, a unique capability most jitter analysis tools cannot do. Jitter can be broken down into random and deterministic components and visualization tools such as jitter tracks and histograms provide valuable insight.

Flexible DDR Measurements

DDR-specific measurement parameters provide an easy way to perform a quantitative analysis of system performance. Display up to 12 measurements for pre-compliance, debug, and system bring-up.

COMPREHENSIVE DDR PHYSICAL LAYER ANALYSIS

The DDR Debug Toolkit provides test, debug and analysis tools for the entire DDR design cycle, making it the ultimate DDR analysis solution.

1. Eye Diagrams Analysis

Depending upon the measurement view, eye diagrams are filtered to display all acquired Read or Write unit intervals (UI). Each view and the reference view can display two eye diagrams, allowing for a maximum of ten eye diagrams to be analyzed simultaneously. Eye diagrams from the same measurement views can be overlaid to show critical timing information.

2. Eye Mask Testing

Select a standard defined mask or choose a custom mask for specialized testing. Mask failures are highlighted to show the exact points where failures occur.

3. Jitter Track Analysis

Display Time Interval Error (TIE) jitter track to view how jitter in the system is changing as a function of time. This analysis will clearly show if there are any time correlated jitter effects such as jitter modulation.

4. Jitter Histogram Analysis

A histogram of the TIE data provides a quick way to clearly determine if jitter aggressors are causing non-Gaussian distributions or long tails.

5. Bathtub Curve

The bathtub curve is a standard plot used to understand the degree to which an eye diagram is closed due to jitter at a given bit error ratio (BER).

6. Eye Measurement Table

Display up to 8 standard eye measurements simultaneously. Use parameters such as eye height and eye width to perform a quantitative assessment of how performance varies across all enabled views.

7. Jitter Measurements Table

Total jitter (Tj) can be separated into deterministic jitter (Dj) and random jitter (Rj) and can be further classified as Duty Cycle Distortion (DCD). Peak-Peak and RMS jitter are available as alternative jitter calculation methods. All jitter can be calculated in time or UI. Results are tabulated for all enabled measurement views.

8. DDR Measurements Table

Enable up to 12 DDR specific measurements at a time to provide a quick overview of system performance for all active views. Configure each measurement to show advanced statistics (min, max, mean, count) and select the measurement source.

9. Completely Integrated Toolset

DDR Debug Toolkit waveform displays and calculations are a completely integrated part of the oscilloscope analysis toolset. Any DDR Debug Toolkit function can be displayed with any other channel acquisition, math function, or measurement parameter on the oscilloscope grid.

POWERFUL DDR DEBUG CAPABILITIES

The bursted nature of DDR signals makes it very different than most serial data communication standards. As a result, the traditional oscilloscope-based methods and algorithms for measuring jitter and analyzing system performance are not capable of measuring DDR signals. The DDR Debug Toolkit uses jitter algorithms which have been tailored for bursted DDR signals. Built-in DDR measurement parameters provide various JEDEC compliance measurements which are important for debugging and characterizing DDR systems.

Read/Write Burst Separation with a Push of a Button

Automatically separate Read and Write bursts with the DDR Debug Toolkit, eliminating the time-consuming process of manual burst identification and simplifying the analysis of DDR system performance and validation. Bursts can be separated based on DQ-DQS phase or based on the command bus when used in conjunction with the HDA125.

DDR Jitter Analysis

Bursted DDR signals create undesirable complications and challenges for traditional serial data analysis and jitter tools preventing analysis of DQ, DQS and address signals. Jitter parameters including Tj, Rj, and Dj are calculated across all active DDR measurement views. To gain a deeper understanding of the jitter distribution, traditional displays such as TIE histograms, TIE track, and bathtub curves are available.

DDR-Specific Parameters

With a toolbox of parameters specific to DDR it is simple to quickly configure insightful measurements for validation, characterization, and debug. Up to 12 configurable measurements can be displayed and analyzed simultaneously across all active measurement views. For each measurement, advanced statistics such as min, max, mean, and number of measurement instances can be displayed and easily located with the searchable zoom feature.

EXTENSIVE EYE DIAGRAM TESTING

An eye diagram is one of the easiest ways to gain a quick understanding of DDR system performance. The DDR Debug Toolkit leverages Teledyne LeCroy's industry leading serial data analysis algorithms and eye diagram rendering tools to provide a unique way to view DDR system performance.

View Up to 10 Eye Diagrams Simultaneously

Any DQ, DQS or command/address signal can be tested against a standard or a custom defined mask. Enabling mask failure indicators will automatically identify any mask violations and locate the specific UI where any mask violation occurred. Built-in measurements such as eye height, eye width and eye opening are critical to gaining a quantitative understanding of the system performance. With simultaneous eye measurements it is easy to compare performance across multiple testing views.

A complete system view is obtained by assigning measurement views to DQ-Read, DQ-Write, DQS-Read and DQS-Write. The reference view shows the DQ-Write eye while the system was using a different termination scheme.

Four Measurement Views

When configuring a measurement, each view can be independently assigned a signal providing extensive flexibility for analysis. For example, it is simple to setup a comparison of system performance between read and write burst operation across multiple DQ lanes. Simultaneous analysis of up to four measurement views simplifies the measurement process and eliminates concerns about making unsynchronized measurements.

Reference View for Optimization Testing

The reference view allows engineers to easily conduct performance tuning or optimization tests. The user is able to store any view into the reference view, then make a change to their setup to observe a change in any performance characteristics. Measurements can be added or removed from the reference view at any time so there is no need to worry about having all analysis parameters defined at the beginning of testing.

ENHANCED DEBUG CAPABILITY WITH THE HDA125

Command Bus Capture for Full Interface Visibility

Basic debugging and validation of embedded DDR interfaces typically involves analysis of the analog properties of the clock, data (DQ) and strobe (DQS) signals - and Teledyne LeCroy's DDR analysis tools are established industry leaders in this application. But when validation tasks become more complex and problems require deeper insight, the ability to trigger on, acquire and visualize the state of the DDR command bus is invaluable. The HDA125 brings command bus acquisition to Teledyne LeCroy's already comprehensive toolset, providing the ultimate in memory bus analysis capability.

Analyze Bus Activity

The HDA125 enables the unique "bus view" feature of the DDR Debug Toolkit, which brings Teledyne LeCroy's advanced bus analysis feature set to bear on DDR analysis. View bus activity in tabular form, and move time-correlated views to a desired event with the touch of a button. Search for specific events and bus states within the acquired record. Intuitive color overlays and annotations make it easy to identify areas of interest in the acquired analog waveforms.

Trigger on DDR Commands

The ability to trigger on specific states of the command bus becomes an invaluable tool for quick understanding of DDR signal quality. The HDA125's logic triggering combines with the DDR Debug Toolkit's intuitive setup and intelligent software cross-triggering to provide the ultimate DDR triggering system. Persistence maps of read and write bursts provide an easy and fast means of identifying subtle signal-quality problems for further investigation.

SPECIFICATIONS

Common Settings

Protocols	DDR2, DDR3, DDR3L, DDR4, DDR5, LPDDR2, LPDDR3, LPDDR4, LPDDR4X
Speed Grades	200, 266, 333, 400, 466, 533, 667, 800, 933, 1066, 1333, 1600, 1866, 2133, 2400, 2666, 2710, 2933, 3200, 3600, 3733, 4000, 4266, 4400, 4800, 5200, 5420, 5600, 6000, 6400, 6800, 7200, 7600, 8000, 8400, Custom
Vref	Standard (VDD/2), Auto Calculated, or Custom

Measurement View Settings

Number of Measurement Views	4 and 1 reference
Analysis Type	DQ-Read, DQ-Write, DQS-Read, DQS-Write, ADDR, Bus (requires a HDA125)
Second Eye	DQ, DQS, CK
Timing Reference	CK or DQS (only applicabel to DQ-Read and DQ-Write)
Input Signals Sources	Analog Channel, EyeDrII, VirtualProbe, Math, Memory, Zoom

Analysis Tools

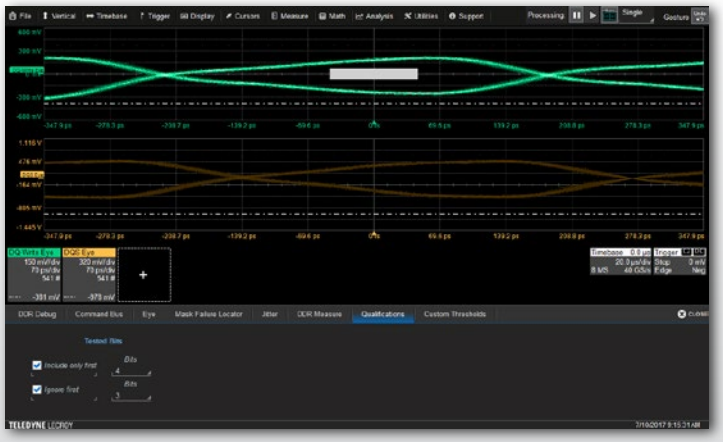
Eye Parameters	Eye Height, Eye Width, Eye Amplitude, Eye Crossing, Mask Hits, Mask Out, One Level, Zero Level
Eye Mask	Standard or Custom. Mask can be automatically horizontally centered in the eye.
Mask Failure Locator	Display mask failures and a total count. Search and zoom to each failure location.
Jitter Plots	TIE Track, TIE Histogram, Cumulative Distribution Function (CDF), Q-FIT Tail Representation, Bathtub
Jitter Parameters	Tj, Rj, Dj, DCD, Pk-Pk, RMS
DDR Measurements	Bursts, Transitions, VH(ac), VH(dc), VL(ac), VL(dc), tDH, tDS, tIH, tIS, tDQSCK, tDQSQ, SlewRise, SlewFall, Vref
DDR Measurement Type	Mean, Max, Min, Number
DDR Measurement Sources	DQ, DQS, CK, ADDR, DQ&DQS, DQS&CK, ADDR&CK, DQ&CK
DDR Measurement Zoom	Zoom to min, max, first or last occurrence of measurement. Alternatively, individually step through each instance.
Analysis Qualifiers	Include only first "N" bits or ignore first "N" bits
Lanescape Comparison Mode	Single: One lane is displayed at a time Dual: Two lanes are selected for display Mosaic: All enabled lanes are displayed

Custom Levels

Customizable Inputs	VDD & VDDQ, Input DC threshold, Vref (DQ), VOH(AC), VOL(AC), Vref(CA)
DQ and CA AC Thresholds	AC300, AC250, AC220, AC200, AC175, AC160, AC150, AC135, AC125, AC120, AC100

Command Bus Analysis (requires an HDA125)

Read/Separation	Command Bus or DQ-DQS phase
Bus Trigger	Read, Write, Read or Write, Bank Activate, Precharge, Refresh, or MRS
Decode Annotation	Color-coded overlays on DQ, DQS, and digital bus
Read and Write Latency	Define Latency in integer numbers from 1 to 30
Command Bus Display	Show Command Bus as expanded or bus view



Analyze Isolated Regions of Bursts

Using built-in configurable qualifiers, all of the analysis in the DDR Debug Toolkit can be gated to include or ignore the first “n” bits. This allows for a deep understanding of how the system is performing under specific conditions. For example, this type of analysis can be used to gain knowledge about how the system is functioning coming out of preamble or exclusively in the middle of burst operation.

ORDERING INFORMATION

DDR Debug Toolkits

	Product Description	Product Code
DDR2	DDR2 and LPDDR2 Debug Toolkit for WaveRunner 9000 Oscilloscopes	WR9K-DDR2-TOOLKIT
	DDR2 and LPDDR2 Debug Toolkit for WavePro HD Oscilloscopes	WPHD-DDR2-TOOLKIT
	DDR2 and LPDDR2 Debug Toolkit for WaveMaster 8 Zi Oscilloscopes	WM8ZI-DDR2-TOOLKIT
	DDR2 and LPDDR2 Debug Toolkit for WaveRunner 10 Zi Oscilloscopes	LM10ZI-DDR2-TOOLKIT
DDR3	DDR3, DDR3L, LPDDR3, DDR2, and LPDDR2 Debug Toolkit for WaveRunner 9000 Oscilloscopes	WR9K-DDR3-TOOLKIT
	DDR3, DDR3L, LPDDR3, DDR2, and LPDDR2 Debug Toolkit for WavePro HD Oscilloscopes	WPHD-DDR3-TOOLKIT
	DDR3, DDR3L, LPDDR3, DDR2, and LPDDR2 Debug Toolkit for WaveMaster 8 Zi Oscilloscopes	WM8ZI-DDR3-TOOLKIT
	DDR3, DDR3L, LPDDR3, DDR2, and LPDDR2 Debug Toolkit for LabMaster 10 Zi Oscilloscopes	LM10ZI-DDR3-TOOLKIT
DDR4	DDR4, LPDDR4/4X, DDR3, DDR3L, LPDDR3, DDR2 and LPDDR2 Debug Toolkit for WavePro HD Oscilloscopes	WPHD-DDR4-TOOLKIT
	DDR4, LPDDR4/4X, DDR3, DDR3L, LPDDR3, DDR2, and LPDDR2 Debug Toolkit for WaveMaster 8 Zi Oscilloscopes	WM8ZI-DDR4-TOOLKIT
	DDR4, LPDDR4/4X, DDR3, DDR3L, LPDDR3, DDR2, and LPDDR2 Debug Toolkit for LabMaster 10 Zi Oscilloscopes	LM10ZI-DDR4-TOOLKIT
DDR5	DDR5, DDR4, LPDDR4/4X, DDR3, DDR3L, LPDDR3, DDR2, and LPDDR2 Debug Toolkit for WaveMaster 8 Zi Oscilloscopes	WM8ZI-DDR5-TOOLKIT
	DDR5, DDR4, LPDDR4/4X, DDR3, DDR3L, LPDDR3, DDR2, and LPDDR2 Debug Toolkit for LabMaster 10 Zi Oscilloscopes	LM10ZI-DDR5-TOOLKIT

Recommended Software Options

Advanced De-embedding, Emulation and Virtual Probing Toolkit	WM8ZI-VIRTUALPROBE LM10ZI-VIRTUALPROBE

Recommended Probes

4 GHz, 2.5 Vpp Differential Probe with ProBus2 Interface	D410-A-PB2
4 GHz, 5 Vpp Differential Probe with ProBus2 Interface	D420-A-PB2
4 GHz, 2.5 Vpp Differential Probe with ProLink Interface	D410-A-PL
4 GHz, 5 Vpp Differential Probe with ProLink Interface	D420-A-PL
6 GHz, 2.5 Vpp Differential Probe with ProBus2 Interface	D610-A-PB2
6 GHz, 5 Vpp Differential Probe with ProBus2 Interface	D620-A-PB2
6 GHz, 2.5 Vpp Differential Probe with ProLink Interface	D610-A-PL
6 GHz, 5 Vpp Differential Probe with ProLink Interface	D620-A-PL
8 GHz Differential Probe with ProBus2 Interface	DH08-PB2
8 GHz Differential Probe with ProLink Interface	DH08-PL
13 GHz Differential Probe with ProLink Interface	DH13-PL
16 GHz Differential Probe with ProLink Interface	DH16-PL
25 GHz Differential Probe with 2.92MM Interface	DH25-2.92MM
DH series solder-in tip 30GHz BW, 3.5Vp-p range	DH-SI
DH series QuickLink adapter, 8 GHz BW	DH-QL

Recommended High-speed Mixed Signal Solutions

12.5 GS/s High-speed Digital Analyzer with 9ch 8 GHz QuickLink leadset	For WaveMaster 8 Zi-B: HDA125-09-LBUS For LabMaster 10 Zi-A:HDA125-09-SYNC

DDR Protocol	Recommended Bandwidth	Recommended Oscilloscope	Recommended Probe (Qty 3 or 4)
DDR2/ LPDDR2 (All Speeds)	≥4 GHz	WaveRunner 9404	D410-A-PB2 / D420-A-PB2
		WavePro HD 4 - 8 GHz models	D410-A-PB2 / D420-A-PB2
		SDA 8 Zi-B 4 - 30 GHz models	D410-A-PL / D420-A-PL
DDR3 / LPDDR3 (1600 MT/s or less)	≥6 GHz	WavePro HD 6 - 8 GHz models	D610-A-PB2 / D620-A-PB2
		SDA 8 Zi-B 6 - 30 GHz models	D610-A-PL / D620-A-PL
DDR3/ LPDDR3 (1866 MT/s or more) **DDR3L** (All Speeds)	≥8 GHz	WavePro 804HD	DH08-PB2
		SDA 8 Zi-B 8 - 30 GHz models	DH08-PL + DH-SI tip
DDR4/ LPDDR4/4X (All Speeds)	≥13 GHz	SDA 8 Zi-B 13 - 30 GHz models	DH13-PL + DH-SI tip
		LabMaster 10 Zi-A All models	DH25-2.92MM + DH-SI tip
DDR5 (All Speeds)	≥16 GHz	SDA 8 Zi-B 16 - 30 GHz models	DH16-PL + DH-SI tip
		LabMaster 10 Zi-A All models	DH25-2.92MM + DH-SI tip

Need Compliance Testing?

QualiPHY™

QualiPHY is designed to reduce the time, effort, and specialized knowledge needed to perform compliance testing on high-speed serial buses.

- Support for DDR2/3/4 and LPDDR2/3/4/4X
- Performs each measurement in accordance with the JEDEC standard
- Guides the user through each test setup
- Compares each measured value with the applicable specification limits
- Fully documents all results
- QualiPHY helps the user perform testing the right way — every time!

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Local sales offices are located throughout the world.
Visit our website to find the most convenient location.